IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A ~~nonvolatile memory having a memory transistor and a reference memory transistor,~~ camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

~~read means~~ a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

~~first write means~~ a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

~~second write means~~ a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

2-90 (Canceled)

91. (New) A camera according to claim 1, wherein the first reference voltage is higher than the second reference voltage.

92. (New) A camera according to claim 1, wherein the second reference voltage is higher

than a threshold voltage of the reference memory transistor.

93. (New) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

94. (New) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

95. (New) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

96. (New) A camera according to claim 1, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

97. (New) A camera according to claim 1, wherein the memory transistor and the reference memory transistor store multilevel information.

98. (New) A camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read based on a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

99. (New) A camera according to claim 98, wherein the first reference voltage is higher than the second reference voltage.

100. (New) A camera according to claim 98, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

101. (New) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

102. (New) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

103. (New) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

104. (New) A camera according to claim 98, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

105. (New) A camera according to claim 98, wherein the memory transistor and the reference memory transistor store multilevel information.

106. (New) A camera comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

107. (New) A camera according to claim 106, wherein the first reference voltage is higher than the second reference voltage.

108. (New) A camera according to claim 106, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

109. (New) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

110. (New) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

111. (New) A camera according to claim 106, wherein each of the memory transistor

and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

112. (New) A camera according to claim 106, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

113. (New) A camera according to claim 106, wherein the memory transistor and the reference memory transistor store multilevel information.

114. (New) A camera comprising:

a display portion; and

a nonvolatile memory the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read from a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read from a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

115. (New) A camera according to claim 114, wherein the first reference voltage is higher than the second reference voltage.

116. (New) A camera according to claim 114, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

117. (New) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

118. (New) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

119. (New) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

120. (New) A camera according to claim 114, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control

gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

121. (New) A camera according to claim 114, wherein the memory transistor and the reference memory transistor store multilevel information.

122. (New) A camera comprising:

a display portion: and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a timer;

a first circuit for performing electrical write on the memory transistor for each time when an elapsed time measured by the timer reaches an arbitrarily preset time until a threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor is higher than a first reference voltage; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

123. (New) A camera according to claim 122, wherein the first reference voltage is higher than the second reference voltage.

124. (New) A camera according to claim 122, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

125. (New) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

126. (New) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

127. (New) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

128. (New) A camera according to claim 122, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

129. (New) A camera according to claim 122, wherein the memory transistor and the reference memory transistor store multilevel information.

130. (New) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

131. (New) A mobile information terminal according to claim 130, wherein the first reference voltage is higher than the second reference voltage.

132. (New) A mobile information terminal according to claim 130, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

133. (New) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

134. (New) A mobile information terminal according to claim 130, wherein each of the

memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

135. (New) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

136. (New) A mobile information terminal according to claim 130, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

137. (New) A mobile information terminal according to claim 130, wherein the memory transistor and the reference memory transistor store multilevel information.

138. (New) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read based on a reference voltage of the

reference memory transistor, and a second threshold voltage of the memory transistor, which is read based on a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

139. (New) A mobile information terminal according to claim 138, wherein the first reference voltage is higher than the second reference voltage.

140. (New) A mobile information terminal according to claim 138, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

141. (New) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

142. (New) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

143. (New) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film,

and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

144. (New) A mobile information terminal according to claim 138, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

145. (New) A mobile information terminal according to claim 138, wherein the memory transistor and the reference memory transistor store multilevel information.

146. (New) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory, the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

a reference memory transistor;

a first circuit for electrically reading a threshold voltage of the memory transistor by using a threshold voltage of the reference memory transistor;

a second circuit for performing electrical write on the memory transistor until the threshold voltage of the memory transistor is higher than a first reference voltage; and

a third circuit for performing electrical write on the reference memory transistor until the threshold voltage of the reference memory transistor is higher than a second reference voltage.

147. (New) A mobile information terminal according to claim 146, wherein the first

reference voltage is higher than the second reference voltage.

148. (New) A mobile information terminal according to claim 146, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

149. (New) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

150. (New) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

151. (New) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

152. (New) A mobile information terminal according to claim 146, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

153. (New) A mobile information terminal according to claim 146, wherein the memory transistor and the reference memory transistor store multilevel information.

154. (New) A mobile information terminal comprising:

a display portion; and

a nonvolatile memory the nonvolatile memory comprising:

a unit cell in which multiple memory transistors are connected in series;

reference memory transistor;

a first circuit for performing electrical write on the memory transistor until a first threshold voltage of the memory transistor, which is read from a reference voltage of the reference memory transistor, and a second threshold voltage of the memory transistor, which is read from a first reference voltage of the reference memory transistor belong to a distribution of threshold voltages for same information; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

155. (New) A mobile information terminal a according to claim 154, wherein the first reference voltage is higher than the second reference voltage.

156. (New) A mobile information terminal according to claim 154, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

157. (New) A mobile information terminal according to claim 154, wherein each of the

memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

158. (New) A mobile information terminal a according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

159. (New) A mobile information terminal according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

160. (New) A mobile information terminal according to claim 154, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

161. (New) A mobile information terminal according to claim 154, wherein the memory transistor and the reference memory transistor store multilevel information.

162. (New) A mobile information terminal comprising:

a display portion: and

a nonvolatile memory, the nonvolatile memory comprising:

a memory transistor;

a reference memory transistor;

a timer;

a first circuit for performing electrical write on the memory transistor for each time when an elapsed time measured by the timer reaches an arbitrarily preset time until a threshold voltage of the memory transistor, which is read based on a reference voltage of the reference memory transistor is higher than a first reference voltage; and

a second circuit for performing electrical write on the reference memory transistor until a threshold voltage of the reference memory transistor is higher than a second reference voltage.

163. (New) A mobile information terminal according to claim 162, wherein the first reference voltage is higher than the second reference voltage.

164. (New) A mobile information terminal according to claim 162, wherein the second reference voltage is higher than a threshold voltage of the reference memory transistor.

165. (New) A mobile information terminal a according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a charge accumulating region, and a control gate, and the charge accumulating region is provided between the active region and the control gate and overlaps the control gate.

166. (New) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a floating

gate, and a control gate, and the floating gate is provided between the active region and the control gate and overlaps the control gate.

167. (New) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a nitride film, and a control gate, and the nitride film is provided between the active region and the control gate and overlaps the control gate.

168. (New) A mobile information terminal according to claim 162, wherein each of the memory transistor and the reference memory transistor comprises an active region, a cluster layer, and a control gate, and the cluster is provided between the active region and the control gate and overlaps the control gate.

169. (New) A mobile information terminal according to claim 162, wherein the memory transistor and the reference memory transistor store multilevel information.